A STUDY OF MULTI-STACK SILICON-DIRECT WAFER BONDING FOR MEMS MANUFACTURING

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ABSTRACT

Multi-stack wafer bonding is one of the most promising fabrication techniques for creating three-dimensional microstructures, such as for power MEMS devices. However, there are several bonding issues that MEMS technologists have to face and overcome to successfully build multilayered structures. Among these are: (1) Chemical residues on surfaces to be bonded originating from the fabrication processes prior to bonding, (2) Increased stiffness due to multiple bonded wafers and/or thick wafers, (3) Bonding tool effects, and (4) Defect propagation to other wafer levels after high-temperature annealing cycles. The problems and the solutions presented here are readily applicable to any MEMS project involving the fabrication of multi-stack structures of two or more wafers containing intricate geometries and large etched areas.

INTRODUCTION

During silicon-direct wafer bonding two hydrophobic or hydrophilic silicon surfaces are brought into direct contact and then annealed at high temperature. This approach can be extended to include several wafers for building more complicated structures. Successful demonstrations of multi-stack silicon-direct bonding processes include complex micro-turbine designs which have achieved rotational speeds in excess of 1.2×10^6 *rpm*, micro-rockets and a 6-wafer combustion system that has survived high-temperature operation for several tens of hours [1]. Figure 1 includes detailed views of each of the 6 wafers in a micro-combustor, along with a 3-D schematic of the stack. Given the complexity of bonding six patterned wafers with thickness varying from 450 to 1000 μm and a total stack thickness of ~ 4000 μm, developing this process posed significant challenges. In this paper several bonding issues encountered in multi-stack silicon-direct wafer bonding for MEMS micromanufacturing are examined and practical solutions discussed.

PROCESSING AND BONDING ISSUES

The bonding procedure used in the experiments can be succinctly described as follows: after all wafer etches were completed and the wafers were ready for bonding, the sacrificial silicon dioxide layer was removed using either hydrogen fluoride (HF) or buffered oxide etch (BOE). Since ammonium fluoride (NH_4F) contained in BOE renders the silicon surface rough, resulting in a relatively low

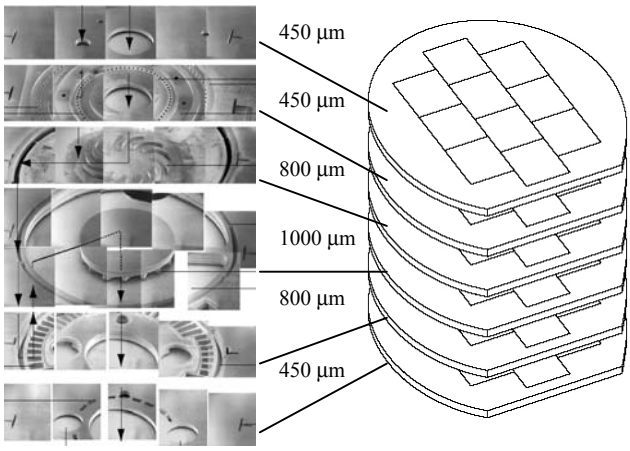


Figure 1. *An example of the 6-wafer combustion wafers prior to bonding along with a 3-D schematic of the stack [1].*

bonding energy, BOE was used only for partially removing any oxide films. Prior to bonding, all wafers were inspected with an optical microscope and prepared for bonding with a standard RCA clean. Wafer alignment and contacting were performed with equipment from Electronic Visions that has been described [2]. The contacting results were examined using an infrared (IR) source in conjunction with a CCD camera. Prior to the high temperature anneal step, the bond is reversible. If the quality of the bond was not deemed acceptable the wafers were debonded and the entire sequence reinitiated with the RCA clean step. Ultimately, the bonded substrates were annealed at 1050°C for 1 hour in nitrogen ambient.

(1) Surface Contamination Issues

While it is possible to demonstrate the successful bonding of several blank, prime silicon wafers (see Figure 2), the same task can be difficult to achieve with processed wafers because of the presence of residual films that contaminate the surfaces to be bonded and can effectively preclude a good bond.

We observed that deleterious residues could originate in any of the wet chemical processing steps. Furthermore, unwanted films could also be deposited on surfaces to be bonded by dry-processing tools (see Figure 3(a)). Since the wafers for multi-stack bonding usually undergo a large number of processing steps care must be exercised throughout the process to avoid surface contamination. For example, the low bonding yield shown in Figure 3(b) was traced back to a carbonaceous residue deposited on the

bottom surface of the substrates during through-wafer deep reactive ion etching (DRIE). All subsequent wafers requiring similar processing steps had a thin (~1000 Å), sacrificial silicon dioxide coating to protect the surfaces of wafers. This protective oxide film was grown thermally and patterned by BOE. In general, SiO_2 films present on the surfaces to be bonded should not be removed until the wafers are ready for bonding. With these additional precautions in place, the bonding of a six-wafer stack in the subsequent build produced a 100% yield (see Figure 3(c)).

(2) Stiffness Related Issues

Multi-stack bonding becomes increasingly more difficult when thick wafers or previously bonded stacks are involved because the stiffness of a sample is proportional to the cube of its thickness. The relevance of this issue becomes apparent during multi-stack bonding because it is necessary for silicon wafers to mate together homogeneously and to conform to the general contour of the surfaces involved. Thus, in the presence of bow or warpage it is more challenging to achieve good, reliable bonds.

Figure 4 illustrates the relevance of stiffness during wafer bonding. The IR image shown in 4(a) is that of a bonded six-wafer stack having a total thickness of 3950 μm. The bonding approach was as follows. First, the bottom three wafers of thicknesses 1000, 800 and 450 μm, respectively (corresponding to levels 4, 5 and 6) were contacted and annealed, resulting in a sample with a thickness of 2250 μm and 13 μm bow across the stack. Subsequently and sequentially levels 3, 2 and 1 (with respective thicknesses of 800, 450, and 450 μm), were mated to the previously bonded three-wafer stack and pressed at 0.3 *bar* for 2 *minutes*. Due to the large stiffness of the 2250 μm thick stack, the bonded area was small and the yield was only one out of 10 possible dies. Predictably, the failing interface was located between the three-wafer bonded stack (with a correspondingly large stiffness) and the wafer corresponding to level 3.

The bond strength increases with time even at room temperature [2]. However, the effect of time in storage can be exploited only when the wafers conform to each other and the gap between them is small enough for the surfaces to attract each other and/or chemical bonds to form. This observation suggests that the bonding process can be promoted by applying, for a sufficiently long time, a large pressure to the contacted surfaces to compensate for the elastic energy induced by each individual wafer bow/warpage.

By extending the pressing time from 2 to 30 *minutes* while applying a pressure of 4 *bar*, it was possible to obtain better results in terms of yield (see Figure 4(b)) when producing a 6-wafer stack. For these relatively short pressing times, a "spring-back" effect was observed after the pressure was released. This effect is indicated in figure 4(b) in the area surrounded by the dashed line.

Further exploring this approach, the pressing time was subsequently extended to 24 *hours* while maintaining the contacting pressure of 4 *bar*. The bonded area increased approximately four times with respect to the first build, with some defects remaining around the edges (see Figure 4(c)) and a yield of 4 good dies out of 10.

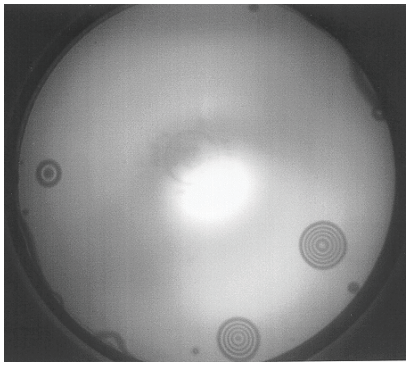


Figure 2. *IR image of a stack of seven-wafers silicon-direct bonded (total thickness: ~5000 μm).*

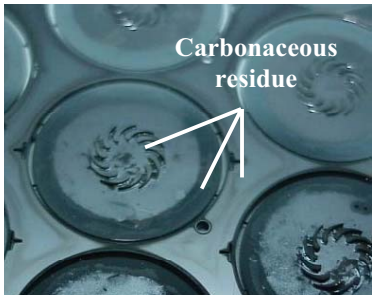
In all the previously described exercises, the contacting under pressure was performed at room temperature. It was always followed by a high-temperature annealing cycle in a quartz furnace with no pressure applied to the 6-wafer stack. It was thought, however, that it could be possible to obtain good results by pressing the samples and increasing the temperature at the same time. The applied pressure would serve to maintain the samples in intimate contact and the increased temperature would increase the bond strength while reducing the spring-back effect. In a subsequent build of a 6-wafer stack the temperature during contacting was maintained at 500 $^{\circ}C$ while applying a pressure of 4 *bar*. The results obtained with this approach are shown in Figure 4(d) after a 4-*hour* thermal press. Compared with Figure 4(c), it was observed that the defects around the edge were diminished, resulting in a high yield of 9 good dies out of 10.

(3) Bonding Tool Effects

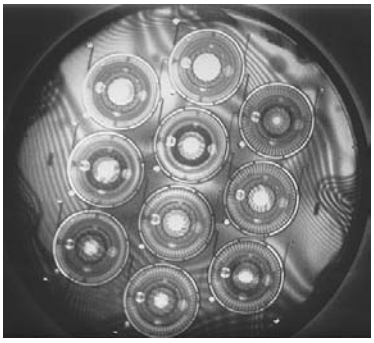
When producing advanced MEMS devices requiring the bonding of multiple wafer stacks, MEMS technologists must be very observant during each step of the production of the wafers and stacks involved as well as on all the tools and fixtures employed. These empirical observations, as shown in Figure 5, consistently revealed an average bow of ~20 μm on bonded pairs of wafers 525 μm thick after they were pressed for 2 *minutes* when applying a pressure of 4 *bar* using a Teflon chuck. However, under the same contacting conditions and using a steel chuck, the measured bow was reduced to ~2 μm. Based on these observations, the exercises described herein where conducted employing the steel bond chuck.

(4) Defect Propagation

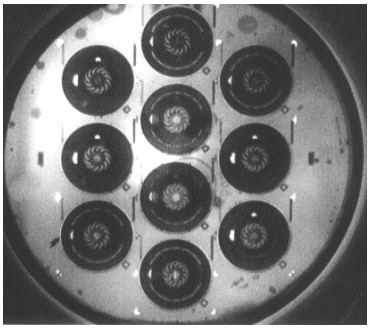
The presence of particulates on surfaces to be bonded as well as the appearance of protrusions that locally distort a wafer surface can both have deleterious effects on yield or preclude additional bonds. For instance, the presence of a 1 μm particle can cause a void as large as 1 *cm* in diameter



(a)



(b)

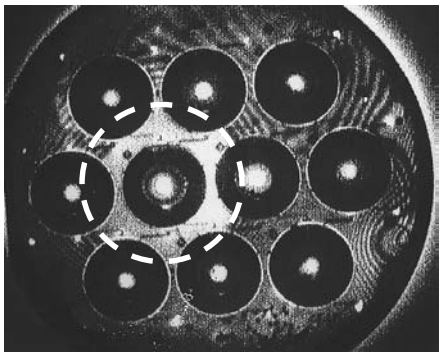


(c)

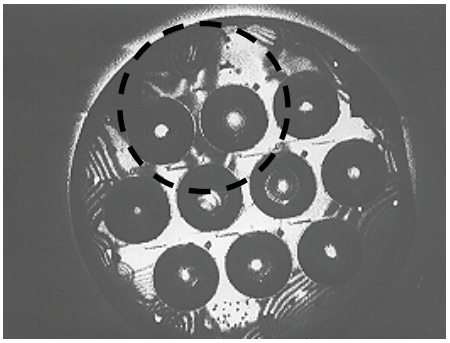
Figure 3. *(a) Carbonaceous residue observed on some surfaces after DRIE, (b) surface contamination produces bonded stacks with low or no yield, and (c) IR image of a bonded 6-wafer stack with a 100% yield.*

when direct-bonding 200 μm thick wafers [2]. Also, annealing cycles performed at high-temperature can cause plastic deformation of the substrates involved due to the expansion of trapped gases in sealed cavities. Specifically, we observed that a cavity of area 1 cm^2 and 1 μm deep located at the interface between two standard 525 μm thick wafers caused a protrusion of ~20 μm on each wafer after annealing for 1 *hour* at 1100^{o}C. This defect in turn precluded additional wafer-level bonding. The best possible solution when forming cavities is to include in the design additional fluidic passages for the cavity to be connected to the external ambient and avoid pressure differentials between the cavity and the outside world.

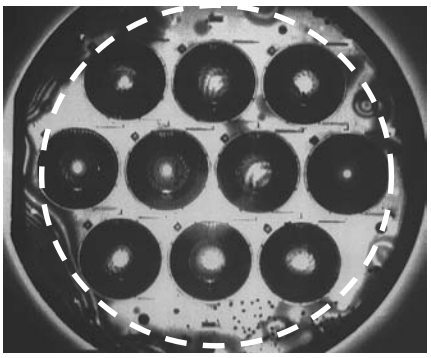
An example depicting the deleterious effect described above can be observed in the IR image of a 5-wafer stack (see Figure 6(a)). *A posteriori* analysis indicated that the source of the defects was located at the interface



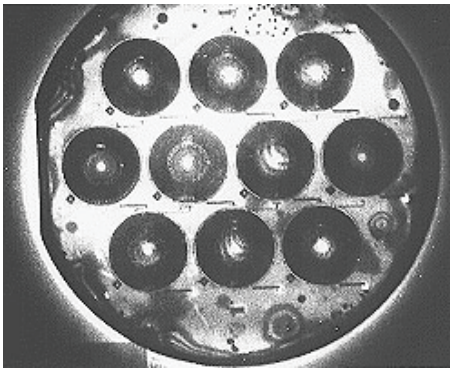
(a)



(b)



(c)



(d)

Figure 4. *Comparison of IR bonding images after (a) 2-minute pressing at 0.3 bar, (b) 30-minute pressing at 4 bar, (c) 24-hour pressing at 4 bar, and (d) 4-hour thermal pressing at 4 bar and 500 °C.*

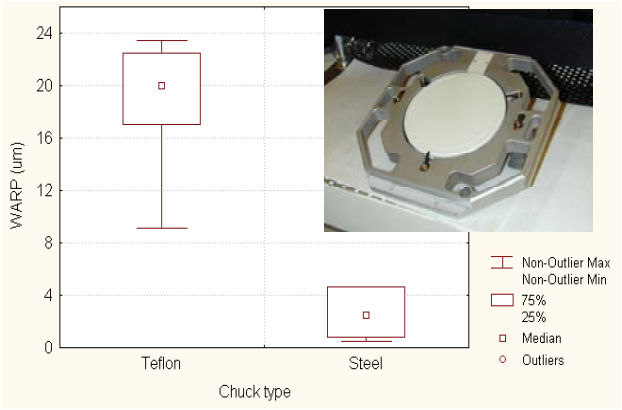


Figure 5. *Effect of chuck types on the warping of wafers.*

between wafers 3 and 4 (see dashed circles in Figure 6(b)). The defects created protrusions on the surface of the fourth wafer that was to be bonded to the subsequent fifth wafer. However, the aforementioned protrusions prevented additional bonds to be performed. The magnified view of the resulting unbonded region shown in Figure 6(b) was caused by propagated defects such as that shown in the surface image of Figure 6(c).

As it was in the case of particulates, propagated defects and protrusions can be much larger than the source defects precluding the completion of complicated structures or producing devices with unacceptable yields. Finally, protrusion removal using CMP may not be compatible with particularly complex structures. Therefore, for projects involving multi-stack bonding, the issue of defect propagation must be taken into account prior to the annealing process.

CONCLUSIONS

We have discussed several bonding issues encountered when manufacturing multi-stack silicon structures for three-dimensional MEMS applications. (a) We observed that undesirable residues could contaminate the surfaces of wafers that have undergone several process steps. This problem can be minimized by utilizing sacrificial SiO_2 coatings. 100% bonding yields have been obtained. (b) Due to the large stiffness of the stacks or wafers being employed, the presence of bow or warpage can preclude a good bond. This problem can be solved by increasing the applied pressure during contacting to compensate for the stiffness encountered and it can also be alleviated by pressing and heating the samples at the same time. (c) The characteristics of the bonding tools must be taken into consideration. Thus, larger wafer bows were observed when using Teflon chucks compared to steel fixtures. (d) Plastic deformation during high-temperature annealing cycles transmits the defects from a bonding interface to a

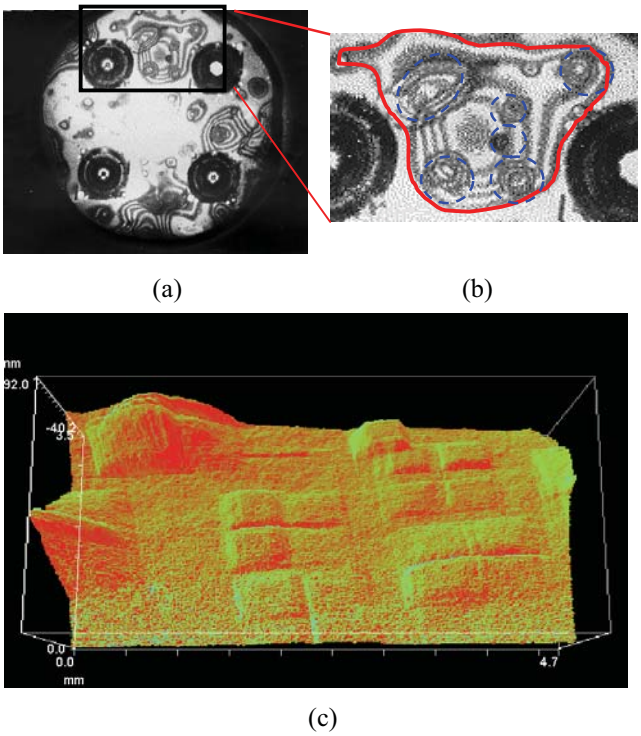


Figure 6 *(a) IR image of 5-wafer stack, (b) close-up view of a protrusion, and (c) surface image of the propagated defects.*

peripheral one. This issue can be averted by a judicious design of the cavities to be connected to the outside world. The issues and solutions presented here are readily applicable to the fabrication of any multi-wafer MEMS project involving intricate geometries and large etched areas.

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